

CLAIMS

What is claimed is:

- 1 1. A computer system, comprising:
2 a processor capable of executing multiple threads;
3 an I/O controller coupled to said processor;
4 an I/O device coupled to said I/O controller; and
5 a main system memory coupled to said processor;
6 wherein said processor processes a program in a main thread that includes instructions
which cause the processor to spawn a pre-execution thread in which at least a
portion of the same program executes, said pre-execution thread runs concurrently
with the main thread, but ahead of the main thread in program order.
- 7 2. The computer system of claim 1 wherein said instructions that cause the pre-execution
8 thread to be spawned include a start instruction which causes a pre-execution thread to start and a
9 stop instruction which causes the pre-execution thread to stop.
- 10 3. The computer system of claim 2 wherein said start instruction includes a value designating
11 the location in the program where the pre-execution thread is to start running.
- 12 4. The computer system of claim 1 wherein the pre-execution thread encounters a cache miss
13 condition for a memory reference but the main thread does not encounter a cache miss condition
when that same memory reference is processed by the main thread.

1 5. The computer system of claim 1 wherein said processor determines whether sufficient
2 hardware resources are available before spawning said pre-execution thread.

1 6. The computer system of claim 1 wherein said processor ignores exception conditions
2 generated during the pre-execution thread.

1 7. The computer system of claim 1 wherein said processor does not permit a store instruction
2 in the pre-execution thread to modify main system memory contents.

8. The computer system of claim 1 wherein said processor does not permit any store
instruction in the pre-execution thread to modify main system memory contents.

9. The computer system of claim 1 further including a buffer into which pre-execution thread
stores data is written to make such store data available to pre-execution thread load instructions.

1 10. A processor, comprising:
2 a fetch unit capable of fetching instructions from a plurality of threads;
3 a program counter coupled to said fetch unit;
4 an instruction cache coupled to said fetch unit;
5 a data cache coupled to said instruction cache;
6 wherein said processor processes a program in a first thread that includes instructions
7 which cause the processor to spawn a second thread in which at least a portion of

8 the same program also executes, said second thread runs concurrently with the first
9 thread, but ahead of the first thread in program order.

1 11. The processor of claim 10 wherein said instructions that cause a second thread to be
2 spawned include a start instruction which causes the second thread to start and a stop instruction
3 which causes the second thread to stop.

1 12. The processor of claim 11 wherein said start instruction includes a value designating the
2 location in the program where the second thread is to start running.

1 13. The processor of claim 10 wherein the second thread encounters a cache miss condition for
2 a memory reference but the first thread does not encounter a cache miss condition when that same
3 memory reference is processed by the first thread.

1 14. The processor of claim 10 wherein said processor determines whether sufficient hardware
2 resources are available before spawning said second thread.

1 15. The processor of claim 10 wherein said processor ignores exception conditions generated
2 during the second thread.

1 16. The processor of claim 10 wherein said processor does not permit a store instruction in the
2 second thread to modify data cache contents.

1 17. The processor of claim 10 wherein said processor does not permit any store instruction in
2 the second thread to modify data cache contents.

1 18. The processor of claim 10 further including a buffer into which pre-execution thread store
2 data is written to make such store data available to pre-execution thread load instructions.

1 19. A method of running a program in a processor, comprising:
2 (a) inserting pre-execution thread instructions in the program;
3 (b) spawning a pre-execution thread when designated by the inserted instructions; and
4 (c) running said pre-execution thread concurrently with a main thread wherein both the
5 pre-execution and the main threads include instructions from the same program, the
6 pre-execution thread running ahead of the main thread.

1 20. The method of claim 19 further including stopping the pre-execution thread when
2 designated by the inserted instructions in (a).

1 21. The method of claim 19 further including copying register contents associated with the
2 main thread to registers used by the pre-execution thread.

1 22. The method of claim 19 further including determining whether sufficient hardware
2 resources are available to spawn the pre-execution thread.

1 23. The method of claim 19 further including ignoring all exception conditions generated
2 during the pre-execution thread.

1 24. The method of claim 19 further including not permitting a store instruction in the pre-
2 execution thread to modify memory contents.

1 25. The method of claim 19 further including copying the contents of at least one register to
2 memory to make such contents available to the pre-execution thread.

26. The method of claim 19 further including writing pre-execution store data into a buffer that
can be accessed by a pre-execution load instruction.

27. The method of claim 19 further including not permitting any store instruction in the pre-
execution thread to modify memory contents.

1 28. The method of claim 19 wherein (a) includes inserting a start instruction which causes the
2 processor to start the pre-execution thread.

1 29. The method of claim 19 wherein the start instruction specifies a location in the program at
2 which the pre-execution thread is to start running.

1 30. The method of claim 19 wherein (a) includes inserting a stop instruction which causes the
2 processor stop the pre-execution thread.

- 1 31. A processor, comprising:
2 a fetch unit capable of fetching instructions from a plurality of threads;
3 a program counter coupled to said fetch unit;
4 an instruction cache coupled to said fetch unit;
5 a data cache coupled to said instruction cache;
6 wherein said processor pre-executes instructions from a main thread.
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32. The processor of claim 31 wherein a pre-execution thread is caused to be spawned to pre-execute said instructions by an instruction in the main thread.
33. The processor of claim 31 wherein a pre-execution thread spins on a variable that is set to a predetermined value by the main thread when there are instructions to pre-execute.
34. The processor of claim 31 wherein the processor ceases pre-executing instructions when a program counter is encountered that exceeds a range.
35. The processor of claim 31 wherein the processor ceases pre-executing instructions when the main thread catches up to the pre-executing instructions.
36. The processor of claim 31 wherein the processor ceases pre-executing instructions when the number of pre-executing instructions exceeds a limit.